Patrick J. French, Professor
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Biography: Professor P. J. French was born in Rochford, England, in 1960. He received his B.Sc. in mathematics and M.Sc. in electronics from Southampton University, UK, in 1981 and 1982, respectively. He obtained his Ph.D. in 1986, also from Southampton University, by the work on the piezoresistive effect of polycrystalline silicon.
He then worked at TU Delft, on the Royal Society European Exchange Programme, investigating new flip-flop sensor structures. In 1988 he joined Nissan Motor Company, Yokosuka, Japan, and investigated sensor technologies for automotive applications.
He returned to TU Delft in 1991 to begin a three year FOM sponsored fellowship at the Laboratory for Electronic Instrumentation to study micromachining. Since 1994, he is one of the project leaders of this laboratory. His main research interests are silicon technology, mechanical sensors and actuators, MOS-based sensors and process optimisation related to sensors.
In 1999 he was awarded the Antoni van Leeuwenhoek chair. In 2002 he became head of the Electronic Instrumentation laboratory. He was a general co-chairman of IEEE MEMS conference in 2004.

Title of the lecture: “Integrated MEMS: opportunities and pitfalls”

Abstract: The integration of MEMS devices with electronics opens many opportunities for increased functionality. For example, a single-chip device can be fabricated with on-chip self-test, self-calibration, cross-sensitivity compensation and with a standard digital output. This increases reliability and reduces leading to many new applications, including safety critical ones. However, this integration can also lead to problems. Some harsh environments are simply not suitable for electronics and therefore the two parts have to be separated. A greater problem can be the processing. Processing for electronics and MEMS have to be compatible and should be kept as simple as possible to keep down costs and maximise yield. It is for this reason that many companies have opted for a two-chip approach where the process for the MEMS device can be optimised without concern over the electronics. Despite the complications many successful examples of integrated MEMS can be found. Perhaps the most famous is the Analog Devices accelerometer, which combines surface micromachining with CMOS read-out electronics.

When developing the process for integrated MEMS it is important to consider the strategy. This includes not only aspects of processing but also where the processing will be done since some MEMS processes are not compatible with cleanroom used for CMOS. A number of process strategies have been developed. One option is to perform depositions for the MEMS, followed by planarisation, before the IC processing.

With this option it is important that the additional depositions do not contaminate the wafer. If the MEMS processing is done during the IC processing full access to the cleanroom is required and the thermal budget for the micromachining is limited. The limitation is even greater if the micromachining is done after aluminium deposition. However, PECVD and metals are suitable for this strategy. The simplest approach is to use existing layers for the mechanical layer. Although simple, the approach has the problem that the layers in an IC process have not been developed for their mechanical properties and often design strategies are required to compensate for unwanted stress.

The presentation will examine the options for integrated micromachining processes, examining the advantages and disadvantages and the opportunities when successful.